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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/628,772	07/28/2003	Greg E. Scott	884.480US2	5797

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
NAMAZI, MEHDI	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 09/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,772	SCOTT ET AL.	
	Examiner	Art Unit	
	Mehdi Namazi	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/28/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to preliminary amendment filed August 3, 2004.

Specification

2. Applicant is required to update status of parent application on page 1.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-25 is rejected under the judicially created doctrine of double patenting over claims 1-24 of U. S. Patent No. 6,615,329 since the claim, if allowed, would improperly extend the "right to exclude" already granted in the patent.

A question of patentability is raised with respect to representative claims 1-25 of the instant application under the judicially doctrine of "obviousness-type" double patenting with respect to U.S. Patent No. 6,615,329.

More specifically, OPQR maintains that in view of the "obviousness-type" double patenting rational enunciated in Georgia pacific Corp v United States Gypsum Co., 52 USPQ2d 1590, U.S. Court of Appeals Federal Circuit 1999, representative application claims 1-25 merely defines an obvious variation of the invention claimed in US Patent 6,636,950.

Initially it should be noted that the present application is a continuation application of parent patent 6,636,950 having the same inventive entity. The Assignee in both applications is Intel Corporation. The entire disclosures of the instant application and patent number 6,636,950 are identical.

Claims 1-24 of the patent is compared to claims 1-25 of instant application in the table below.

Instant Application	Patent
1. An article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing:	1. A method of controlling access to a protected area of a memory including a first set of instructions, comprising:
detecting an attempted write operation to a protected area of a memory including a first set of instructions;	detecting an attempted write operation to the protected area;
using a second set of instructions not located in the memory to determine that an authorization flag not located in the	using a second set of instructions not located in the memory to determine that an authorization flag not located in the

memory has been set by the first set of instructions; and if the authorization flag has been set, enabling the attempted write operation.	memory has been set by the first set of instructions; and if the authorization flag has been set, enabling the attempted write operation.
2. The article of claim 1, wherein detecting an attempted write operation to the protected area includes: detecting activation of at least two signal lines connected to the memory.	2. The method of claim 1, wherein detecting an attempted write operation to the protected area includes detecting activation of a plurality of signal lines connected to the memory.
3. The article of claim 2, wherein detecting activation of the at least two signal lines connected to the memory includes: simultaneously detecting activation of at least one address line connected to the memory and at least one access enabling line connected to the memory.	3. The method of claim 2, wherein detecting activation of a plurality of signal lines connected to the memory includes simultaneously detecting activation of a plurality of address lines connected to the memory and at least one access enabling line connected to the memory.
4. The article of claim 1, wherein detecting an attempted write operation to the protected area includes: activating an interrupt line connected to a processor.	4. The method of claim 1, wherein detecting an attempted write operation to the protected area includes activating an interrupt line connected to a processor.
5. The article of claim 1, wherein the second set of instructions and the	5. The method of claim 1, wherein the second set of instructions is located in an

authorization flag are located in another memory.	other memory, and wherein the authorization flag is also located in the other memory.
6. The article of claim 1, wherein the second set of instructions is located in another memory, and wherein the authorization flag is not located in the other memory.	6. The method of claim 1, wherein the second set of instructions is located in an other memory, and wherein the authorization flag is not located in the other memory.
7. The article of claim 1, wherein using a second set of instructions not located in the memory to determine that an authorization flag not located in the memory has been set by the first set of instructions includes: determining a value of a bit not located in the memory.	7. The method of claim 1, wherein using a second set of instructions not located in the memory to determine that an authorization flag not located in the memory has been set by the first set of instructions includes determining a value of a bit not located in the memory.
8. The article of claim 1, wherein enabling the attempted write operation includes: activating at least one access enabling line connected to the memory.	8. The method of claim 1, wherein enabling the attempted write operation includes activating at least one access enabling line connected to the memory.
9. The article of claim 8, wherein detecting an attempted write operation to the protected area includes: simultaneously	9. The method of claim 8, wherein detecting an attempted write operation to the protected area includes simultaneously

detecting activation of at least one address line connected to the memory and the at least one access enabling line connected to the memory.	detecting activation of a plurality of address lines connected to the memory and the at least one access enabling line connected to the memory.
10. The article of claim 1, wherein the data, when accessed, results in the machine performing: detecting that the attempted write operation has been completed.	10. The method of claim 1, further including: detecting that the attempted write operation has been completed.
11. The article of claim 10, wherein detecting that the attempted write operation has been completed includes: detecting an occurrence of a software interrupt.	11. The method of claim 10, wherein detecting that the attempted write operation has been completed includes detecting an occurrence of a software interrupt.
12. The article of claim 10, wherein the data, when accessed, results in the machine performing: disabling a future write operation to the protected area.	12. The method of claim 10, further including: disabling a future write operation to the protected area.
13. The article of claim 12, wherein disabling the future write operation to the protected area includes: deactivating at least one access enabling line connected	13. The method of claim 12, wherein disabling a future write operation to the protected area includes deactivating at least one access enabling line connected

to the memory.	to the memory.
14. The article of claim 1, wherein the data, when accessed, results in the machine performing: otherwise, if the authorization flag has not been set, refraining from enabling the attempted write operation.	14. The method of claim 1, further including: otherwise, if the authorization flag has not been set, refraining from enabling the attempted write operation.
15. An apparatus, comprising: a first memory having a protected area including a first set of instructions to set a state of a flag and to write to the protected area, the first memory including an access enabling line; a write detection module having an output coupled to an interrupt to indicate an attempt to write to the protected area; and a second memory including a second set of instructions in operational	15. A memory access control circuit, comprising: a first memory having a protected area including a first set of instructions to set a state of a flag and to write to the protected area, the first memory including an access enabling line; a write detection module having an output to indicate an attempt to write to the protected area; **a processor module connected to the access enabling line, the processor including a first interrupt connected to the write detection module;** and a second memory including a second set of instructions in operational

communication with the interrupt, the second set of instructions adapted to determine the state of the flag.	communication with the first interrupt, the second set of instructions adapted to determine the state of the flag.
16. The apparatus of claim 15, further comprising: a third memory in operational communication with the second set of instructions, wherein the third memory includes the flag.	16. The memory access control circuit of claim 15, further including: a third memory in operational communication with the second set of instructions, wherein the third memory includes the flag.
17. The apparatus of claim 15, wherein the write detection module and the second memory are included in a single integrated module.	17. The memory access control circuit of claim 15, **wherein the processor module**, the write detection module, and the second memory are included in a single integrated module.
18. The apparatus of claim 15, wherein the first memory comprises a flash memory.	19. The memory access control circuit of claim 15, wherein the first memory is a flash memory
19. An apparatus, comprising: a network interface; and a memory access control circuit operationally connected to the network interface, the memory access control circuit including a first memory	20. A set-top client, comprising: a network interface; and a memory access control circuit operationally connected to the network interface, the memory access control circuit including, a first memory

having a protected area including a first set of instructions to set a state of a flag and to write to the protected area, the first memory including an access enabling line, a write detection module having an output coupled to an interrupt to indicate an attempt to write to the protected area, and (claim 20) (claim 21) a second memory including a second set of instructions in operational communication with the interrupt, the second set of instructions adapted to determine the state of the flag.	having a protected area including a first set of instructions to set a state of a flag and to write to the protected area, the first memory including an access enabling line; a write detection module having an output to indicate an attempt to write to the protected area; a processor module connected to the access enabling line, the processor including a first interrupt connected to the write detection module; and a second memory including a second set of instructions in operational communication with the first interrupt, the second set of instructions adapted to determine the state of the flag.
23. A system, comprising: a server; and an apparatus capable of being coupled to the server, the apparatus including	24. A networked system, comprising: a server; a network connected to the server; and a set-top client connected to the

(claims 24-25)	network, the set-top client including, a network interface; and a memory access control circuit operationally connected to the network interface, the memory access control circuit including,
a first memory having a protected area including a first set of instructions to set a state of a flag and to write to the protected area, the first memory including an access enabling line, a write detection module having an output to indicate an attempt to write to the protected area, and	a first memory having a protected area including a first set of instructions for to set a state of a flag and to write to the protected area, the first memory including an access enabling line; a write detection module having an output to indicate an attempt to write to the protected area; **a processor module connected to the access enabling line, the processor including a first interrupt connected to the write detection module;** and
a second memory including a second set of instructions in operational communication with the write detection module, the second set of instructions, upon execution, capable of determining the state of the flag.	a second memory including a second set of instructions in operational communication with **the first interrupt**, the second set of instructions adapted to determine the state of the flag.

Claims 1-25 of the instant application is anticipated by claims 1-24 of that patent. Claims 1-25 of the instant application therefore is not patently distinct from the earlier patent claims and as such is unpatentable for obvious-type double patenting.

Under the rules of GATT/NAFTA for implementation of the 20 years term effective June 8, 1995, the term of the affronted U.S. patent ends the same date as the instant application. Therefore, patent protection rights due application from U.S. Patent No. 6,615,329 B2 cannot be timewise extended by issuance of the instant application even without a properly drafted terminal disclaimer in this case. **However in lieu of the cancellation of the claims or abandonment of the instant application, applicants must overcome this question of patentability by submission of a paper that at least addresses the "enforceability/common ownership" provision of a terminal disclaimer referred to in 37 CFR 1.321 (C) (3).**

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mehdi Namazi whose telephone number is 571-272-4209. The examiner can normally be reached on Monday-Friday 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mehdi Namazi
Patent Examiner

September 21, 2004